DETAILED ACTION

1. Applicant's amendments dated December 11, 2008 and March 5, 2009 respectively, responding to the Office action mailed August 11, 2008 provided in the rejection of claims 1-7 and 9-67, wherein claims 1, 2, 25, 29, 53, and 65 have been amended.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with Mr. Michael J. Swope (Reg. No. 38,041) on April 7, 2009 to obviate any potential 35 U.S.C 101 and 35 U.S.C 112, second paragraph issues, and to place the claims in the condition for allowance.

4. The application has been amended as follows:

IN THE CLAIMS,

Please amend claims 25, 29, and 65 as follows:

25. (Currently amended)

A method for a guest operating system to determine whether it is running on a virtualized processor or running directly on a hardware processor, said method comprising:

executing a synthetic instruction for returning a value representing an identity for the central processing unit, wherein said synthetic instructions are configured to cause at least one exception to be trappable by a virtualization layer, and wherein said synthetic instructions are illegal to said processor architecture;

wherein said synthetic instruction is configured to be executed from any privileged level;

when a value is returned, using synthetic instructions;

~~wherein said synthetic instructions are configured to cause at least one exception to be trappable by a virtualization layer, and wherein said synthetic instructions are illegal to said processor architecture;~~ and

not using synthetic instructions when an exception occurs.

29. (Currently amended)

A system for processing synthetic instructions on x86 processor architectures and their equivalents, comprising:

a processor having an x86 architecture;

a memory coupled to said processor by way of a bus;

a subsystem stored in said memory for trapping said synthetic instructions issued by a guest operating system after said synthetic instructions cause an exception in the x86 processor; and

a subsystem stored in said memory for processing said synthetic instructions for the guest operating system;

wherein at least one synthetic instruction of said synthetic instructions is configured to enable direct execution within ring 0 layer of privilege.

65. (Currently amended)

A system for processing synthetic instructions when executing on x86 processor architectures ~~and their equivalents, including but not limited to the IA32 architecture~~, said system comprising:

a processor having an x86 architecture;

a memory coupled to said processor by way of a bus;

computer readable instructions stored in said memory that when executed by said processor cause removing, replacing, or supplementing instances of one or more of the following predefined instructions in [[the]] a guest operating system: PUSH CS, PUSH SS, MOV from SS, CALLF, VERR, VERW, and LAR with synthetic instructions that are configured to cause at least one exception to be trappable by a virtualization layer, and wherein said synthetic instructions are illegal to said processor architecture.

- **END OF AMENDMENT –**

Allowable Subject Matter

5. Claims 1-7 and 9-67 (renumbered as 1-66) are allowed.

6. The following is an examiner's statement of reasons for allowance:

As pointed out in REMARKS of the amendment that "… *Devine* simply does not teach the synthetic instructions as claimed … *Devine* teaches binary translation and not the use of synthetic instructions … *Devine* does not remove, replace or supplement guest operating instructions with instructions that are 'illegal to said architecture' …" (recited on page 14, first non-full paragraph)

Further, as pointed out by Applicant(s), the prior art of record fails to teach and/or suggest:

"… for processor virtualization in processor architectures comprising:
identifying in the instruction set of a guest operating system one or more predefined instructions, wherein said one or more predefined instructions do not cause the processor to trap execution of said one or more predefined instructions;
removing, replacing, or supplementing the identified one or more predefined instructions with at least one synthetic instruction that causes at least one exception to be trappable by a virtualization program, wherein said synthetic instructions are illegal to said architecture; and
using at least one of said synthetic instructions to enable direct execution on a physical processor of instructions issued by said guest operating

system; wherein said at least one of said synthetic instructions is executed from within guest kernel code", as recited in independent claim 1 and similarly recited in independent claims 24, 27, 28, 51, 64, 65, and 66.

Furthermore, the claimed invention compensates for the shortcomings in x86 processor architectures by introducing "synthetic instructions" that cause a trap and thereby provide an opportunity for the virtual machine (VM) to process the instructions safely. By using instructions that are "illegal" to the x86 architecture but which are nonetheless understandable by a virtual machine, the present method uses synthetic instructions to perform well-defined actions in the virtual machine that are otherwise problematic when performed by traditional instructions executed on an x86 processor and thereby provides much-improved processor virtualization for x86 processor system (recited in paragraph [0010])

7. Claims 2-23, 25-26, 29-50, and 52-63 are considered allowable by virtue of their dependence on allowable independent claims 1, 24, 28, and 51 respectively.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben C. Wang whose telephone number is (571) 270-1240. The examiner can normally be reached on 8:00-5:30 (EST/EDT), Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ben C Wang/
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Examiner, Art Unit 2192

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192